REMARKS/ARGUMENTS

Claims 1-16, 18-20, 22-37, and 55-59 are pending in this application. By this Amendment, Applicant AMENDS Claim 1 and ADDS Claim 59.

Applicant greatly appreciates the allowance of Claims 2, 3, 5, 7, 9, 11, 13, 18-20, 23, 26, 27, 30, 31, 35-37, 57, and 58 by the Examiner.

The Examiner rejected Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55, and 56 under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi (U.S. 2002/0102823) in view of Murakami et al. (U.S. 2002/0068388). The Examiner rejected Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55, and 56 under 35 U.S.C. §103(a) as being unpatentable over Inoue et al. (U.S. 5,693,959) in view of Murakami et al. The Examiner rejected Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55, and 56 under 35 U.S.C. §103(a) as being unpatentable over Takahashi et al. (U.S. 2003/0080384) in view of Murakami et al. The Examiner rejected claims 24, 25, and 32 under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi et al. in view of Murakami et al., and further in view of Yamazaki et al. (U.S. 2002/0100937).

Applicant respectfully traverses the rejections of Claims 1, 4, 6, 8, 10, 14-16, 22, 24, 25, 28, 29, 32, 55, and 56.

Applicant has amended Claim 1 to recite:

> A semiconductor device, comprising:
> a thin film transistor including a semiconductor layer that includes a channel region, a source region, and a drain region;
> a gate insulating film provided on the semiconductor layer; and
> a gate electrode for controlling a conductivity of the channel region; wherein
> **the gate electrode includes an inclined side surface;**
> **a surface of the semiconductor layer includes a protruding portion located under the inclined side surface of the gate electrode;**
> a cross-section of the gate electrode includes first and second opposing sides that are parallel to each other and a third side that is not parallel to any other side of the cross-section of the gate electrode; and
> a side surface inclination angle of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer. (emphasis added)

In the first paragraph on page 3, the fourth paragraph on page 5, and the fifth

paragraph on page 7 of the outstanding Office Action, the Examiner admitted that Yamaguchi, Inoue et al., and Takahashi et al., respectively, fail to teach or suggest a gate electrode having the cross-section as required by Applicant's Claim 1. The Examiner relied upon Murakami et al. to allegedly cure this deficiency in each of Yamaguchi, Inoue et al., and Takahashi et al. In the last paragraph on page 3, the first full paragraph on page 6, and the first full paragraph on page 8 of the outstanding Office Action, the Examiner alleged that it would have been obvious to use the doping implantation process of Marukami et al. in one of the processes of Yamaguchi et al., Inoue et al., and Takahashi et al. for the purpose of modifying the devices of Yamaguchi et al., Inoue et al., and Takahashi et al. by providing regions with different doping concentrations to form Lightly Doped Drain (LDD) regions that are effective in reducing the OFF current value.

First, Applicant respectfully submits that the Examiner has failed to provide proper motivation for modifying each of the devices of Yamaguchi et al., Inoue et al., and Takahashi et al. to have the tapered gate electrode of Murakami et al. because the tapered electrode is not necessary in the formation of the LDD regions. That is, even if one of ordinary skill in the art wanted to provide the devices of Yamaguchi et al., Inoue et al., and Takahashi et al. with LDD regions, the Examiner has failed to explain why it would be necessary to use tapered electrodes to provide the LDD regions.

Thus, Applicant respectfully submits that the Examiner has failed to provide proper motivation for modifying the devices of each of Yamaguchi et al., Inoue et al., and Takahashi et al. in view of Murakami et al.

Second, Applicant amended Claim 1 to recite the feature of "a protruding portion located under the inclined side surface of the gate electrode." With this feature, Applicant has been able to prevent the formation of a parasitic transistor and to prevent a humped curve in the off-state leak current (see, for example, paragraph nos. [0077] and [0078] of the originally filed Specification).

Each of Yamaguchi, Inoue et al., and Takahashi et al. teach the use of a gate electrode having a rectangular cross-section. That is, each of Yamaguchi, Inoue et al., and Takahashi et al. fails to teach or suggest a gate electrode having an inclined side

surface as required by Applicant's Claim 1. Thus, Yamaguchi, Inoue et al., and Takahashi et al. clearly fail to teach or suggest the feature of "a protruding portion located under the inclined side surface of the gate electrode" as recited in Applicant's Claim 1.

Murakami et al. does teach the use of a gate electrode having an inclined or tapered side surface. However, Murakami et al. fails to teach or suggest that the surface of the semiconductor layer has a protruding portion as required by Applicant's Claim 1. Thus, Murakami et al. clearly fail to teach or suggest the feature of "a protruding portion located under the inclined side surface of the gate electrode" as recited in Applicant's Claim 1.

Further, neither Murakami et al. nor any prior art reference of record provide any motivation or suggestion to modify the devices of Yamaguchi, Inoue et al., and Takahashi et al. such that "a protruding portion [on the surface the semiconductor layer is] located under the inclined side surface of the gate electrode" as recited in Applicant's Claim 1.

Thus, Applicant respectfully submits that Yamaguchi, Inoue et al., Takahashi et al., and Murakami et al., either alone or in combination, fail to teach or suggest the feature of "a protruding portion located under the inclined side surface of the gate electrode" as recited in Applicant's Claim 1.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 1 under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi in view of Murakami et al., the rejection of Claim 1 under 35 U.S.C. §103(a) as being unpatentable over Inoue et al. in view of Murakami et al., and the rejection of Claim 1 under 35 U.S.C. §103(a) as being unpatentable over Takahashi et al. in view of Murakami et al.

The Examiner has relied upon Yamazaki et al. to allegedly cure various deficiencies in Yamaguchi et al. and Murakami et al. However, Yamazaki et al. fails to teach or suggest the feature of "a protruding portion located under the inclined side surface of the gate electrode" in combination with the other features recited in Applicant's Claim 1.

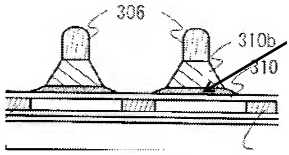
Applicant has added new Claim 59 that recites:

> A semiconductor device, comprising:
> a thin film transistor including a semiconductor layer that includes a channel region, a source region, and a drain region;
> a gate insulating film provided on the semiconductor layer; and
> a gate electrode arranged to control a conductivity of the channel region; wherein
> a surface of the semiconductor layer includes a protruding portion;
> a cross-section of the gate electrode includes first and second opposing sides that are parallel to each other and a third side that is not parallel to any other side of the cross-section of the gate electrode;
> the gate electrode has side surface inclination angles that change within a range according to the height of the gate electrode;
> **the range of the side surface inclination angles of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer**; and
> **the inclination angle of the protruding portion of the semiconductor layer is about 30° to about 70°**. (emphasis added)

With respect to Yamaguchi, Inoue et al., Takahashi et al., and Yamazaki et al., Applicant's Claim 59 recites the feature of "the range of the side surface inclination angles of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer." Each of Yamaguchi, Inoue et al., Takahashi et al., and Yamazaki et al. teach the use of a gate electrode having a rectangular cross-section. That is, each of Yamaguchi, Inoue et al., Takahashi et al., and Yamazaki et al. fails to teach or suggest a gate electrode having more than one side surface inclination angle as required by Applicant's Claim 59. Thus, Applicant respectfully submits that Yamaguchi, Inoue et al., Takahashi et al., and Yamazaki et al. clearly fail to teach or suggest the feature of "the range of the side surface inclination angles of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer" as recited in Applicant's Claim 59.

With respect to Murakami et al., Applicant's Claim 59 additionally recites the feature of "the inclination angle of the protruding portion of the semiconductor layer is about 30° to about 70°." Murakami et al. teaches the use of a gate electrode having two side surface inclination angles. However, as shown in the below partial, marked-up **Fig. 4b** of Murakami et al., relied upon by the Examiner, the bottom portion of the gate

electrode **310b** (**315b** not shown below) has a side surface inclination angle much below 30°.



Thus, Applicant respectfully submits that Murakami et al. fails to teach or suggest the features of "the range of the side surface inclination angles of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer" and "the inclination angle of the protruding portion of the semiconductor layer is about 30° to about 70°" as recited in Applicant's Claim 59.

Accordingly, Applicant respectfully submits that a rejection of Claim 59 over Yamaguchi, Inoue et al., Takahashi et al., Yamazaki et al., and Murakami et al., either alone or in combination, would be improper.

Accordingly, Applicant respectfully submits that the prior art of record, applied alone or in combination, fails to teach or suggest the unique combination and arrangement of elements recited in Claim 1 of the present application. Claims 4, 6, 8, 10, 14-16, 22, 24, 25, 28, 29, 32, 55, and 56 depend upon Claim 1 and are therefore allowable for at least the reasons that Claim 1 is allowable. The Examiner has allowed Claims 2, 3, 5, 7, 9, 11, 13, 18-20, 23, 26, 27, 30, 31, 35-37, 57, and 58.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

To the extent necessary, Applicant petitions the Commissioner for a TWO-month extension of time, extending to September 18, 2006, the period for response to the Office Action dated April 18, 2006.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Dated: September 18, 2006

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